

Amendments to the Claims

No claims are added.

Claim 58 is canceled.

Claims 21-57 are pending.

21. (Previously presented) A system, comprising:
a random access memory device;
a first signal line coupled to the random access memory device, the first
signal line to carry a first signal;
a second signal line coupled to the random access memory device, the
second signal line to carry a second signal; and
a memory controller coupled to the first signal line and the second signal line,
wherein the memory controller includes a delay locked loop to generate the first
signal, wherein the first signal is used to transmit data to the random access memory
device, the delay locked loop to receive the second signal such that the second signal
is used to sample read data provided by the memory device.

22. (Previously presented) The system as recited in claim 21,
wherein the memory controller includes a driver such that the first signal is used to
transmit data to the memory device by way of the driver.

23. (Previously presented) The system as recited in 21, wherein the
memory controller includes a sampler to sample the read data using the second
signal.

1
2 24. (Previously presented) The system as recited in claim 21, further
3 comprising:

4 a first delay element coupled in a feedback path of the delay-locked loop to
5 change a phase difference between the second signal and a reference clock signal
6 by a first time period.

7
8 25. (Previously presented) The system as recited in claim 24, further
9 comprising:

10 a second delay element outside the feedback path of the delay-locked loop
11 to receive the second signal, and
12 to delay the first signal relative to the second signal by the first time
13 period.

14
15 26. (Previously presented) The system of claim 21, further
16 including a clock generator to generate the second signal, wherein the second
17 signal propagates from the clock generator to the memory controller.

18
19 27. (Previously presented) The system of claim 26, wherein the second
20 signal is terminated after being received by the memory controller.

21
22 28. (Previously presented) The system of claim 21, wherein the first
23 signal is a clock signal and the second signal is a clock signal.
24
25

1 29. (Previously presented) The system as recited in claim 21,
2 wherein the delay-locked loop further includes a phase detector to identify phase
3 differences between the second signal and the reference clock signal.

4
5 30. (Previously presented) The system as recited in claim 29,
6 wherein the phase detector is a zero phase detector.

7
8 31. (Previously presented) The system as recited in claim 29,
9 wherein the phase detector is an integration sampler to integrate the first signal
10 with respect to the reference clock signal.

11
12 32. (Previously presented) The system as recited in claim 21,
13 wherein the delay-locked loop further includes a 180 degree phase shift circuit to
14 adjust a phase of the second signal.

15
16 33. (Previously presented) The system as recited in claim 32, wherein
17 the 180 degree phase shift is accomplished by switching over the first signal line
18 and the second signal line.

19
20 34. (Previously presented) The system as recited in claim 21,
21 wherein first data of the read data is sampled on a rising edge of the second signal
22 and second data of the read data is sampled on a falling edge of the second signal.
23
24
25

1 35. (Previously presented) The system as recited in claim 21, wherein
2 the delay lock loop generates a receive clock using the second signal, wherein the
3 receive clock is used to sample read data by way of the second signal.

4
5 36. (Previously presented) The system of claim 35, wherein the delay
6 locked loop generates the receive clock such that a phase of the receive clock is
7 aligned with a phase of the second signal.

8
9 37. (Previously presented) A method of operation in a memory
10 controller comprising:

11 generating a first signal using a single delay-locked loop wherein the first
12 signal is used to time data transmission;

13 changing a phase difference between the first signal and a reference signal
14 by a first time period using a second delay element outside the feedback path of the
15 delay-locked loop circuit; and

16 receiving a second signal to be delayed relative to the first signal by the first
17 time period using a first delay element in a feedback path of the delay-locked loop,
18 wherein the second signal is used to time data reception.

19
20 38. (Previously presented) The method as recited in claim 37,
21 further comprising transmitting data by way of a driver.

22
23 39. (Previously presented) The method as recited in 37, further
24 comprising sampling the read data using the second signal.

25

1 40. (Previously presented) The method as recited in claim 37,
2 further comprising changing a phase difference between the second signal and a
3 reference clock signal by a first time period.

4
5 41. (Previously presented) The method as recited in claim 40,
6 further comprising delaying the first signal relative to the second signal by
7 the first time period.

8
9 42. (Previously presented) The method of claim 37, further comprising
10 generating the second signal from a clock generator and propagating the second
11 signal to a memory controller.

12
13 43. (Previously presented) The method of claim 42, further comprising
14 terminating the second signal after the second signal is received by the memory
15 controller.

16
17 44. (Previously presented) The method of claim 37, wherein the first
18 signal is a clock signal and the second signal is a clock signal.

19
20 45. (Previously presented) The method as recited in claim 37,
21 further comprising identifying phase differences between the second signal and the
22 reference clock signal.

23
24 46. (Previously presented) The method as recited in claim 45,
25 further comprising detecting a zero phase difference.

1
2 47. (Previously presented) The method as recited in claim 45,
3 further comprising integrating the first signal with respect to the reference clock
4 signal.

5
6 48. (Previously presented) The method as recited in claim 37,
7 further comprising adjusting a phase of the second signal by 180 degrees.

8
9 49. (Previously presented) The method as recited in claim 48, further
10 comprising switching over the first signal line and the second signal line to effect
11 the 180 degree phase shift.

12
13 50. (Previously presented) The method as recited in claim 37, wherein
14 first data of the read data is sampled on a rising edge of the second signal and
15 second data of the read data is sampled on a falling edge of the second signal.

16
17 51. (Previously presented) The method as recited in claim 37, further
18 comprising generating a receive clock using the second signal, wherein the receive
19 clock is used to sample read data by way of the second signal.

20
21 52. (Previously presented) The method of claim 51, further comprising
22 generating the receive clock such that a phase of the receive clock is aligned with a
23 phase of the second signal.

24
25 53. (Previously presented) A system, comprising:

1 an electronic data store;

2 a controller for the electronic data store, including:

3 a delay-locked loop to receive a second signal, wherein the delay-
4 locked loop includes:

5 a first delay element coupled in a feedback path of the delay-
6 locked loop, wherein the first delay element changes a phase difference between
7 the second signal and a reference clock signal by a first time period, and

8 a second delay element outside the feedback path to receive
9 the second signal and output a first signal that is delayed relative to the second
10 signal by the first time period; and

11 a phase detector to determine phase differences between the second
12 signal and the reference clock signal.

13
14 54. (Previously presented) The system as recited in claim 53,
15 wherein the phase detector comprises a zero phase detector.

16
17 55. (Previously presented) The system as recited in claim 53,
18 wherein the delay-locked loop further includes a 180 degrees phase shifter.

19
20 56. (Previously presented) The system as recited in claim 53,
21 wherein the first and second signals provide timing for address multiplexing
22 operations of the electronic data store.

1 57. (Previously presented) The system as recited in claim 53, further
2 comprising an integration sampler to integrate the first signal with respect to the
3 reference clock signal.

4
5 58. (Canceled)
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25